Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	49	("5862385" "5379393" "6002875" "5630097" "5689679" "5963972" "6317874" "5848275" "6742179" "6249880" "5689712" "6006033" "6668307" "5493660" "5787494" "5276851" "5230045" "5761722" "4587610" "5038278" "5317711" "5978888" "5983322" "6026470" "6098152" "6240500" "5860095" "5317718" "5530958" "5897660" "5893150" "5274811" "5797026" "6052700" "6223228" "6223228" "6230263" "6349365" "5664135" "5664193" "5787302" "5826054" "5852741" "5862398" "5878267" "6131152" "5369753" "5640532" "5678020" "5701503").pn.	US-PGPUB; USPAT	OR	ON	2004/11/12 08:57
S2	63	speculative adj store	US-PGPUB; USPAT	OR	ON	2004/11/12 09:46
S3	0	speculative adj store with (control near dependen$4)	US-PGPUB; USPAT	OR	ON	2004/11/12 09:47
S4	5821	(control near dependen$4)	US-PGPUB; USPAT	OR	ON	2004/11/12 09:47
S5	117	(control near dependen$4) with branch	US-PGPUB; USPAT	OR	ON	2004/11/12 09:47
S6	7	(control near dependen$4) with branch with (remov$3 or eliminat$3)	US-PGPUB; USPAT	OR	ON	2004/11/12 09:59
S8	21	speculat$3 with stor$3 with (predicated or conditional)	US-PGPUB; USPAT	OR	ON	2004/11/12 10:14
S9	2258	717/140-161.ccls.	US-PGPUB; USPAT	OR	ON	2004/11/12 10:07
S10	3815	speculation	US-PGPUB; USPAT	OR	ON	2004/11/12 10:07
S11	67	S9 and S10	US-PGPUB; USPAT	OR	ON	2004/11/12 10:07
S12	43019	(predicated or conditional)	US-PGPUB; USPAT	OR	ON	2004/11/12 10:13
S13	44	S11 and S12	US-PGPUB; USPAT	OR	ON	2004/11/12 10:08
S14	46618	(predicat$3 or conditional)	US-PGPUB; USPAT	OR	ON	2004/11/12 10:13
S15	44	S13 and S14	US-PGPUB; USPAT	OR	ON	2004/11/12 10:13
S16	0	S13 not S15	US-PGPUB; USPAT	OR	ON	2004/11/12 10:13
S17	468	speculat$3 near stor$3	US-PGPUB; USPAT	OR	ON	2004/11/12 10:16

S18	4	S13 and S17	US-PGPUB; USPAT	OR	ON	2004/11/12 10:14
S19	84	speculat$3 adj stor$3	US-PGPUB; USPAT	OR	ON	2004/11/12 10:17
S20	4	S13 and S18	US-PGPUB; USPAT	OR	ON	2004/11/12 10:43
S21	12	"address jamming"	US-PGPUB; USPAT	OR	ON	2004/11/12 10:59
S22	4	(("5999738") or ("6513109")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/12 11:48
S23	184	"compensation code"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 11:49
S24	409	(717/159-161).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/12 11:50
S25	11	S23 and S24	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 11:50
S26	17	("4567574" | "5107418" | "5542075" | "5557761" | "5613121" | "5625835" | "5758051" | "5790862" | "5805894" | "5943499" | "6038657" | "6094713" | "6108770" | "6128775" | "6139199" | "6151704" | "6243864").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2004/11/12 11:59
S27	1	("6516463").URPN.	USPAT	OR	ON	2004/11/12 12:34
S28	21	"partially predicated"	USPAT	OR	ON	2004/11/12 12:37
S29	29	"partially predicated"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 13:35
S30	8	S29 not S28	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 12:38

S31	2	"partial predication"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 12:39
S32	50	"if-conversion"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 12:39
S33	1388	(712/233-240).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/12 13:34
S34	7	S32 and S33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 13:34
S35	58	partial$2 adj predicat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 13:41
S36	1777	S24 or S33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 13:35
S37	5	S35 and S36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 13:35
S38	17748	speculat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 13:41
S39	12	S35 and S38	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 13:42
S40	17	("4567574" | "5107418" | "5542075" | "5557761" | "5613121" | "5625835" | "5758051" | "5790862" | "5805894" | "5943499" | "6038657" | "6094713" | "6108770" | "6128775" | "6139199" | "6151704" | "6243864").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2004/11/12 14:00

S41	0	"Method for removing dependent store-load pair from critical path".ti.	US-PGPUB; USPAT; USOCR	OR	ON	2004/11/12 14:00
S42	80	(assembly or assembler) same relative with addressing	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/12 15:57

Terms used **speculative store** Found **41,173** of **838,400**

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1 The store-load address table and speculative register promotion
Matthew Postiff, David Greene, Trevor Mudge
December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**
Full text available: pdf(170.83 KB) ps(2.97 MB) Publisher Site
Additional Information: full citation, references, citings, index terms

2 Architectural support for scalable speculative parallelization in shared-memory multiprocessors
Marcelo Cintra, José F. Martínez, Josep Torrellas
May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2
Full text available: pdf(253.29 KB)
Additional Information: full citation, abstract, references, citings, index terms

Speculative parallelization aggressively executes in parallel codes that cannot be fully parallelized by the compiler. Past proposals of hardware schemes have mostly focused on single-chip multiprocessors (CMPs), whose effectiveness is necessarily limited by their small size. Very few schemes have attempted this technique in the context of scalable shared-memory systems. In this paper, we present and evaluate a new hardware scheme for scalable speculative parallelization. This de ...

3 Register promotion by sparse partial redundancy elimination of loads and stores
Raymond Lo, Fred Chow, Robert Kennedy, Shin-Ming Liu, Peng Tu
May 1998 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1998 conference on Programming language design and implementation**, Volume 33 Issue 5
Full text available: pdf(1.76 MB)
Additional Information: full citation, abstract, references, citings, index terms

An algorithm for register promotion is presented based on the observation that the circumstances for promoting a memory location's value to register coincide with situations where the program exhibits partial redundancy between accesses to the memory location. The recent SSAPRE algorithm for eliminating partial redundancy using a sparse SSA representation forms the foundation for the present algorithm to eliminate redundancy among memory accesses, enabling us to achieve both computational and li ...

4 Sentinel scheduling: a model for compiler-controlled speculative execution
Scott A. Mahlke, William Y. Chen, Roger A. Bringmann, Richard E. Hank, Wen-Mei W. Hwu, B. Ramakrishna Rau, Michael S. Schlansker

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1 A comparison of full and partial predicated execution support for ILP processors
Scott A. Mahlke, Richard E. Hank, James E. McCormick, David I. August, Wen-Mei W. Hwu
May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture**, Volume 23 Issue 2
Full text available: pdf(1.48 MB) Additional Information: full citation, abstract, references, citings, index terms

One can effectively utilize predicated execution to improve branch handling in instruction-level parallel processors. Although the potential benefits of predicated execution are high, the tradeoffs involved in the design of an instruction set to support predicated execution can be difficult. On one end of the design spectrum, architectural support for full predicated execution requires increasing the number of source operands for all instructions. Full predicate support provides for the most fle ...

2 Compilation: The impact of if-conversion and branch prediction on program execution on the Intel® Itanium™ processor
Youngsoo Choi, Allan Knies, Luke Gerke, Tin-Fook Ngai
December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**
Full text available: pdf(1.06 MB) Additional Information: full citation, abstract, references, citings
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The research community has studied if-conversion for many years. However, due to the lack of existing hardware, studies were conducted by simulating code generated by experimental compilers. This paper presents the first comprehensive study of the use of predication to implement if-conversion on production hardware with a near-production compiler. To better understand trends in the measurements, we generated binaries at three increasing levels of if-conversion aggressiveness. For each level, we ...

3 Multimedia and graphics: Enhancing loop buffering of media and telecommunications applications using low-overhead predication
John W. Sias, Hillery C. Hunter, Wen-mei W. Hwu
December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**
Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, citings
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Media- and telecommunications-focused processors, increasingly designed as deeply pipelined, statically-scheduled VLIWs, rely on loop buffers for low-overhead execution of simple loops. Key loops containing control flow pose a substantial problem---full predication has a high encoding overhead, and partial predication techniques do not support if-conversion, the transformation of general acyclic control flow into predicated blocks. Using a

Terms used **partial predicate speculative** Found **2,362** of **838,400**

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1 A comparison of full and partial predicated execution support for ILP processors

Scott A. Mahlke, Richard E. Hank, James E. McCormick, David I. August, Wen-Mei W. Hwu

May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture**, Volume 23 Issue 2

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One can effectively utilize predicated execution to improve branch handling in instruction-level parallel processors. Although the potential benefits of predicated execution are high, the tradeoffs involved in the design of an instruction set to support predicated execution can be difficult. On one end of the design spectrum, architectural support for full predicated execution requires increasing the number of source operands for all instructions. Full predicate support provides for the most fle ...

2 Integrated predicated and speculative execution in the IMPACT EPIC architecture

David I. August, Daniel A. Connors, Scott A. Mahlke, John W. Sias, Kevin M. Crozier, Ben-Chung Cheng, Patrick R. Eaton, Qudus B. Olaniran, Wen-mei W. Hwu

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture**, Volume 26 Issue 3

Full text available: pdf(1.60 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Explicitly Parallel Instruction Computing (EPIC) architectures require the compiler to express program instruction level parallelism directly to the hardware. EPIC techniques which enable the compiler to represent control speculation, data dependence speculation, and predication have individually been shown to be very effective. However, these techniques have not been studied in combination with each other. This paper presents the IMPACT EPIC Architecture to address the issues involved in design ...

3 Compilation: The impact of if-conversion and branch prediction on program execution on the Intel® Itanium™ processor

Youngsoo Choi, Allan Knies, Luke Gerke, Tin-Fook Ngai

December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.06 MB) Publisher Site Additional Information: full citation, abstract, references, citings

The research community has studied if-conversion for many years. However, due to the lack of existing hardware, studies were conducted by simulating code generated by experimental compilers. This paper presents the first comprehensive study of the use of predication to implement if-conversion on production hardware with a near-production compiler. To better understand trends in the measurements, we generated binaries at three increasing levels of